Claims

[c1] An integrated circuit structure comprising:
a substrate;
first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors; and
second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, and second spacers adjacent said first spacers.

[c2] The integrated circuit structure in claim 1, wherein said second spacers are only adjacent said first spacers that are adjacent said second gate conductors, and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

[c3] The integrated circuit structure in claim 1, further comprising an etch stop layer positioned between said first spacers and said second spacers, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors.

[c4] The integrated circuit structure in claim 1, further comprising:
first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors; and
second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors.

[c5] The integrated circuit structure in claim 4, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

[c6] The integrated circuit structure in claim 4, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

[c7] The integrated circuit structure in claim 1, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-

type field effect transistors (PFETs).

[c8] An integrated circuit structure comprising:
a substrate;
first-type transistors on said substrate, wherein said first-type transistors comprise first gate conductors and first spacers adjacent said first gate conductors; and
second-type transistors on said substrate, wherein said second-type transistors comprise second gate conductors, said first spacers adjacent said second gate conductors, an etch stop layer on said first spacers, and second spacers on said etch stop layer.

[c9] The integrated circuit structure in claim 8, wherein said second spacers are only adjacent said first spacers that are adjacent said second gate conductors and said second spacers are not adjacent said first spacers that are adjacent said first gate conductors.

[c10] The integrated circuit structure in claim 8, wherein said etch stop layer is only on said first spacers that are adjacent said second gate conductors and said etch stop layer is not on said first spacers that are adjacent said first gate conductors.

[c11] The integrated circuit structure in claim 8, further comprising:
first-type impurity implants in areas of said substrate adjacent said first spacers of said first gate conductors; and
second-type impurity implants in areas of said substrate adjacent said second spacers of said second gate conductors.

[c12] The integrated circuit structure in claim 11, wherein said first-type impurity is spaced closer to said first gate conductors than said second-type impurity is spaced from said second gate conductors.

[c13] The integrated circuit structure in claim 11, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

[c14] The integrated circuit structure in claim 8, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

[c15] A method of simultaneously forming different types of transistors on a substrate, said method comprising:
forming first spacers adjacent gate conductors on said substrate;
implanting a first-type impurity in portions of said substrate adjacent said first spacers of first-type transistors;
forming second spacers adjacent said first spacers such that all of said gate conductors have double spacers;
implanting a second-type impurity in portions of said substrate adjacent said second spacers of second-type transistors;
removing said second spacers from said first-type transistors; and
siliciding exposed areas of said substrate and said gate conductors not covered by said first spacers and said second spacers.

[c16] The method in claim 15, further comprising, before forming said first spacers, implanting an extension impurity in regions of said substrate adjacent said gate conductors.

[c17] The method in claim 15, wherein said first-type impurity is spaced closer to said gate conductors than said second-type impurity.

[c18] The method in claim 15, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

[c19] The method in claim 15, wherein said first-type transistors comprise n-type field effect transistors (NFETs) and said second-type transistors comprise p-type field effect transistors (PFETs).

[c20] The method in claim 15, further comprising forming an etch stop layer between said first spacers and said second spacers, wherein said etch stop layer prevents said process of removing said second spacers from affecting said first spacers.

[c21] A method of simultaneously forming different types of transistors on a single substrate, said method comprising:
forming first spacers adjacent gate conductors on said substrate;
forming a first mask over regions of said substrate to be occupied by second-type transistors;

implanting a first-type impurity in portions of said substrate adjacent said first spacers of first-type transistors;
removing said first mask;
forming an etch stop layer on all of said first spacers, on said substrate, and on exposed portions of said gate conductors;
forming second spacers on said etch stop layer such that all of said gate conductors have double spacers;
forming a second mask over regions of said substrate to be occupied by said first-type transistors;
implanting a second-type impurity in portions of said substrate adjacent said second spacers of said second-type transistors;
removing said second mask;
forming a third mask over regions of said substrate to be occupied by said second-type transistors;
removing said second spacers from said first-type transistors;
removing said third mask; and
siliciding exposed areas of said substrate and said gate conductors not covered by said first spacers and said second spacers.

[c22] The method in claim 21, wherein said etch stop layer prevents said process of removing said second spacers from affecting said first spacers.

[c23] The method in claim 21, further comprising, before forming said first spacers, implanting an extension impurity in regions of said substrate adjacent said gate conductors.

[c24] The method in claim 21, wherein said first-type impurity and said second-type impurity comprises source/drain impurities.

[c25] The method in claim 21, wherein said first-type transistors comprise p-type field effect transistors (PFETs) and said second-type transistors comprise n-type field effect transistors (NFETs).